Taylor Cowley

Lab 11: Controlling the LC3 Datapath

June 13 2016

**Preparation (10pts possible)**

* Datapath Verilog file (10pt)

**Procedure (30pts possible)**

* Master TCL file (2pt)
* Wave TCL file (2pt)
* Inactive TCL file (2pt)
* Fetch TCL file (2pt)
* All instruction TCL files (12pt)
* Full Simulation waveform (10pt)

**Anomalies (bugs, problems, and suggestions)(5pts possible)**